WHAT IS CLAIMED IS:

1. A delay circuit, for a semiconductor device, having a plurality of cascade-connected stages that successively delay an input signal, the delay circuit comprising:

a plurality of cascaded-connected delay devices representing instances of a first type of delay unit corresponding to the plurality of stages, respectively;

a plurality of resistance units coupled between a node having a source voltage of varying magnitude Vvar and odd-numbered ones of the plurality of delay devices, respectively; and

a plurality of capacitance units coupled between a node having another voltage Vuni of substantially uniform magnitude relative to Vvar and nodes representing the outputs of the odd-numbered delay devices;

corresponding ones of the plurality of capacitor units and the plurality of resistance units representing instances, respectively, of a second type of delay unit.

2. The delay circuit as claimed in 1, wherein each of the plurality of capacitance units is an MOS-type capacitor.

3. The delay circuit as claimed in 2, wherein each of the plurality of delay devices is an MOS-type inverter.

4. The delay circuit as claimed in 3, wherein Vvar is externally-supplied.

5. The delay circuit as claimed in 1, wherein Vuni < Vvar.

6. The delay circuit as claimed in 1, wherein:

couplings represented by the plurality of resistance units are indirect types of couplings, respectively; and

even-numbered ones of the plurality of delay devices have direct type couplings, respectively, relative to the indirect couplings.

7. A delay circuit, for a semiconductor device, having a plurality of cascade-connected stages that successively delay an input signal, the delay circuit comprising:

a plurality of cascaded-connected delay devices representing instances of a first type of delay unit corresponding to the plurality of stages, respectively;

a plurality of resistance units coupled between a node having a source voltage of varying magnitude Vvar and odd-numbered ones of the plurality of delay devices, respectively; and

a plurality of capacitance units coupled between a node having a first control voltage V1 of substantially uniform magnitude relative to Vvar and nodes representing the outputs of the odd-numbered delay devices; and

a plurality of switch units controlled by a second control voltage V2 of substantially uniform magnitude relative to Vvar and coupled in parallel with the plurality of resistance units between the node having Vvar and the odd-numbered delay devices, respectively;

corresponding ones of the plurality of switch units, the plurality of capacitor units and the plurality of resistance units representing instances, respectively, of a second type of delay unit

8. The delay circuit as claimed in 8, wherein each of the plurality of

capacitance units is an MOS-type capacitor.

9. The delay circuit as claimed in 8, wherein each of the plurality of delay devices is an MOS-type inverter.

10. The delay circuit as claimed in 8, wherein Vvar is externally-supplied.

11. The delay circuit as claimed in 8, wherein Vuni < Vvar.

12. The delay circuit as claimed in 8, wherein:

couplings represented by corresponding ones of the plurality of switching units and the plurality of resistance units are indirect types of couplings, respectively; and

even-numbered ones of the plurality of delay devices have direct type couplings to Vvar, respectively, relative to the indirect couplings.

13. The delay circuit as claimed in claim 8, wherein V2=V1.

14. The delay circuit as claimed in 8, wherein each of the plurality of switch units is an MOS-type transistor.

15. The delay circuit as claimed in claim 8, wherein the plurality of stages has 4 stages.

16. The delay circuit as claimed in claim 1, wherein the plurality of stages has 4 stages.

17. The delay circuit as claimed in claim 1, further comprising switched resistance devices coupled in parallel with the plurality of resistance units between the node having Vvar and the odd-numbered delay devices, respectively, operation of which selectively changes impedances between the node having a source voltage of varying magnitude Vvar and the odd-numbered delay devices, respectively.

18. A delay circuit, for a semiconductor device, having a plurality of cascade-connected stages that successively delay an input signal, the delay circuit comprising:

a plurality of cascaded-connected delay means, corresponding to the plurality of stages, respectively, for respectively delaying signals passed therethrough;

a plurality of resistance means for providing impedances to currents flowing between a node having a source voltage of varying magnitude Vvar and odd-numbered ones of the plurality of delay means, respectively; and

a plurality of capacitance means for providing capacitances between a node having another voltage Vuni of substantially uniform magnitude relative to Vvar and nodes representing outputs of the odd-numbered delay means, respectively;

corresponding ones of the plurality of capacitance means and the plurality of resistance means being operable for providing delays of an RC-type, respectively.

19. The delay circuit as claimed in claim 18, further comprising:

a plurality of switched second resistance means coupled in parallel with

the plurality of first resistance means between the node having Vvar and the odd-numbered delay devices, respectively, and for selectively changing impedances between the node having Vvar and the delay means, respectively.

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